WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

first memory elements to store a first state or a second state according to a change in resistance value, each of said first memory elements comprising one terminal and the other terminal, said first memory elements arranged parallel with each other;

a first wiring connected with said one terminal of each of said first memory elements; and

a second wiring formed in parallel with said first wiring and connected with said other terminal of each of said first memory elements;

wherein said first state or said second state stored in one of selected from said first memory elements is read out by delivering an electric current from one of said first and second wirings via said one of selected from said first memory elements to the other of said first and second wirings.

2. The semiconductor memory device according to claim 1, which further comprises a third wiring disposed opposite said first memory elements with said first or second wirings being interposed therebetween, said third wiring arranged a first direction and said first and second wirings arranged a second direction different from said first direction, said third wiring electrically insulated from said first and second wirings, thereby enabling said first state or said

second state to be written into said one of selected from said first memory elements through said third wiring and one of said first and second wirings.

3. The semiconductor memory device according to claim 2, wherein said third wiring passing over an extension line connecting a junction between said first memory elements and said first wiring with a junction between said first memory elements and said second wiring.

4. The semiconductor memory device according to claim 2, wherein said first and second directions cross each other.

5. The semiconductor memory device according to claim 1, which further comprises a third wiring disposed opposite said first memory elements with said first wiring being interposed therebetween, said third wiring arranged a first direction and said first and second wirings arranged a second direction different from said first direction, said third wiring electrically insulated from said first and second wirings, thereby enabling said first state or said second state to be written into said one of selected from said first memory elements through said third wiring and one of said first and second wirings, said third wiring forming a gate electrode of MISFET.

6. The semiconductor memory device according to claim 5, wherein said third wiring passing over an

extension line connecting a junction between said first memory elements and said first wiring with a junction between said first memory elements and said second wiring.

7. The semiconductor memory device according to claim 5, wherein said first and second directions cross each other.

8. The semiconductor memory device according to claim 2, which further comprises:

second memory elements disposed opposite said first memory elements with said third wiring being interposed therebetween, said second memory elements to store a first state or a second state according to a change in resistance value, each of said second memory elements comprising one terminal and the other terminal, said second memory elements arranged parallel with each other;

a fourth wiring formed in parallel with said first and second wirings and connected with said one terminal of each of said second memory elements, said fourth wiring electrically insulated from said third wiring; and

a fifth wiring formed in parallel with said first and second wirings and connected with said other terminal of each of said second memory elements.

9. The semiconductor memory device according to claim 5, which further comprises:

second memory elements disposed opposite said first memory elements with said second wiring being interposed therebetween, each of said second memory elements comprising one terminal and the other terminal, said one terminal of each of said second memory elements connected with said second wiring, said second memory elements to store a first state or a second state according to a change in resistance value, said second memory elements arranged parallel with each other;

a fourth wiring formed in parallel with said first and second wirings and connected with said other terminal of each of said second memory elements; and

a fifth wiring formed in parallel with said third wiring and disposed opposite said second memory elements with said fourth wiring being interposed therebetween, said fifth wiring electrically insulated from said fourth wiring.

10. The semiconductor memory device according to claim 2, wherein said second wiring comprises a thickness which is thinner than that of said first wiring.

11. The semiconductor memory device according to claim 2, wherein said first wiring comprises a thickness which is thinner than that of said second wiring.

12. The semiconductor memory device according to

claim 1, wherein said first memory elements are a tunneling magneto resistive effect element.

13. The semiconductor memory device according to claim 1, wherein said first memory elements, and said first and second wirings are disposed in a ladder pattern.

14. The semiconductor memory device according to claim 1, which further comprises:

a constant-voltage generating circuit applied a constant voltage to said first or second wirings; and

a grounded circuit grounded said first or second wirings.

15. The semiconductor memory device according to claim 14, wherein said constant-voltage generating circuit is connected with one of said first and second wirings and said grounded circuit is connected with the other of said first and second wirings, said electric current to read out deliver from one of said first and second wirings to the other of said first and second wirings.

16. The semiconductor memory device according to claim 14, wherein said first and second wirings comprises one terminal and the other terminal, said constant-voltage generating circuit being connected with said one terminal and said grounded circuit being connected with said other terminal.

17. The semiconductor memory device according to

claim 14, which further comprises a sense circuit connected with said constant-voltage generating circuit or said grounded circuit.

18. The semiconductor memory device according to claim 1, which further comprises a sense circuit to determine said first and second states on the basis of the magnitude of said electric current.

19. The semiconductor memory device according to claim 2, wherein a current flows through one of said first and second wirings and said third wiring, thereby to write the first state or the second state into said one of selected from said first memory elements.

20. The semiconductor memory device according to claim 2, wherein a value a first current flowing from one of said first and second wirings to the other thereof is stored, a second current flows through one of said first and second wirings and said third wiring, thereby to write the first state or the second state into said one of selected from said first memory elements, a value that the second current comprises when the first state or the second state is written into said one of selected from said first memory elements is stored, and the values of the first and second currents are compared, thereby to determine the first or second states written in said one of selected from said first memory elements and to read the state from said one of selected from said first memory

elements.

21. A method of manufacturing a semiconductor memory device where memory elements are employed to store a first state or a second state according to a change in resistance value, said method comprising:

forming a first insulating film on a semiconductor substrate;

forming a first wiring on said first insulating film;

forming said memory elements on said first wiring;

forming a second insulating film on a region between said memory elements;

forming a second wiring on said memory elements and said second insulating film, said second wiring being parallel with said first wiring;

forming a third insulating film on said second wiring; and

forming a third wiring on said third insulating film to crossed with said first and second wirings, said third wiring passing over an extension line connecting a junction between said memory elements and said first wiring with a junction between said memory elements and said second wiring.

22. A method of manufacturing a semiconductor memory device where memory elements are employed to store a first state or a second state according to a change in resistance value, said method comprising:

forming gate electrodes on a semiconductor substrate;

forming a first insulating film on a region between said gate electrodes and on said gate electrodes;

forming a first wiring on said first insulating film to crossed with said gate electrodes;

forming said memory elements on said first wiring disposed over said gate electrodes;

forming a second insulating film on a region between said memory elements; and

forming a second wiring on said memory elements and said second insulating film, said second wiring being parallel with said first wiring.

23. A method of manufacturing a semiconductor memory device where memory elements are employed to store a first state or a second state according to a change in resistance value, said method comprising:

forming a first insulating film on a semiconductor substrate;

forming a first wiring on said first insulating film;

forming said memory elements on said first wiring, said memory elements being linear and crossed with said first wiring;

forming a second insulating film on a region between said memory elements;

forming a second wiring on said memory elements and said second insulating film, said second wiring being parallel with said first wiring;

etching said memory elements into an island pattern with said second wiring being employed as a mask;

forming a third insulating film on said second wiring; and

forming a third wiring on said third insulating film to crossed with said first and second wirings, said third wiring passing over an extension line connecting a junction between said memory elements and said first wiring with a junction between said memory elements and said second wiring.

24. The method of manufacturing a semiconductor memory device according to claim 21, wherein said memory elements are a tunneling magneto resistive effect element.

25. The method of manufacturing a semiconductor memory device according to claim 23, wherein said memory elements are a tunneling magneto resistive effect element.

26. The method of manufacturing a semiconductor memory device according to claim 22, wherein said memory elements are a tunneling magneto resistive effect element.